

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination MBOUOMBOUO ET AL.	
		Examiner Phallaka Kik	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chu et al., "A Quadratic Programming Approach to Simultaneous Buffer Insertion/Sizing and Wire Sizing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 18, No. 6, June 1999, pp. 787-798.
	V	Chu et al., "A New Approach to Simultaneous Buffer Insertion and Wire Sizing", 1997 IEEE/ACM International Conference on Computer-Aided Design, 09 November 1997, pp. 614-621.
	W	Chung et al., "Optimal Buffered Clock Tree Synthesis", Proceedings of Seventh Annual IEEE International ASIC Conference and Exhibit, 19 September 1994, pp. 130-133.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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